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Design and Optimization of an Inverter for a One-Megawatt Ultra-Light Motor Drive

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Mohammad M. Qasim*, David M. Otten[†], Zoltán S. Spakovszky [‡],
Jeffrey H. Lang [§], James L. Kirtley Jr. [¶] and David J. Perreault [‖]

Massachusetts Institute of Technology, Cambridge, MA, 02139

This paper presents the design and optimization of a 1-MW inverter for a high-speed, high-specific-power motor drive. The proposed inverter consists of ten 100-kW inverter sets distributed around the periphery of the machine to drive ten separate sets of three-phase open-ended windings. Each inverter set consists of three single-phase full-bridge inverters each of which drives an open-ended phase winding. The use of three single-phase full-bridge inverters for each inverter set yields an improved specific power as compared to either the three-phase bridge inverter or the active neutral-point clamped (ANPC) inverter in the target application. The proposed inverter system is co-designed and co-optimized with a 1-MW permanent magnet machine and associated thermal management system. Experimental results demonstrating the performance of a 100-kW inverter set are provided. The air-cooled inverter set operates at 720 V_{dc}, 73.5 $A_{ac,rms}$ per phase and 80 kHz device switching frequency, and achieves 53.4 kW/kg specific power and $> 98\%$ efficiency.

I. Introduction

$\mathbf{T}$HE design of light and efficient MW-class high-speed motor drives for aircraft applications is presently receiving considerable attention. Advances in the specific power (i.e. power-to-mass ratio or active-mass power density) of such motor drives including their power electronics are central to the future of hybrid and fully-electric aircraft. Some of the state-of-the-art research in MW-class high-specific-power inverters for this application (including that presented in this paper) is summarized in Table 1.

Other notable research into high-power-density, high-efficiency, converters (< 1-MW) for aircraft electric propulsion is reported in [4–6]. In [4], the authors demonstrated a 9.7-kW air-cooled GaN-based inverter phase leg comprising two interleaved nine-level flying capacitor multilevel inverters (9L-FCML) with 17 kW/kg specific power and 98.6% efficiency. The reported 9L-FCML is demonstrated at full power against resistive loads with 1-kV$_{dc}$/380-V$_{ac,rms}$, 120 kHz device switching frequency and 3 kHz fundamental output frequency (modulation frequency ratio of $33.\bar{3}$). Researchers in [5] presented a 100-kW, 1-kV$_{dc}$/474-V$_{ac,rms}$, air-cooled three-level T-type (3L-Ttype) inverter phase leg for aircraft electric propulsion motor drives. The reported phase-leg inverter uses a hybrid combination of IGBT and SiC power modules per switch position and has 24.5 kW/kg specific power and 98.2% efficiency. The inverter was demonstrated at reduced power of 48 kVA with an inductive load and 42 carrier frequency ratio (reduced ac voltage and current of 313-V$_{ac,rms}$/154-A$_{ac,rms}$ and frequency ratio of 28 kHz/0.6 kHz). In [6], a 40-kW Si-MOSFET cryogenically-cooled three-phase three-level active-neutral-point-clamped (3L-ANPC) inverter is developed and demonstrated at full power for aircraft applications. The inverter features 97.8% efficiency, 23.3 kW/kg specific power and is demonstrated with 1-kV$_{dc}$ and 600V$_{ac,rms}$ line-line voltage and $46.\bar{6}$ carrier frequency ratio (140 kHz/3 kHz).*

This paper focuses on the design and optimization of the power conversion system for a 1-MW motor drive, with the inverter and electric machine co-optimized. A topology comparison of two-level and three-level inverters is performed. It is found that while three-phase multilevel inverters can achieve the highest efficiency, they are heavier than two-level inverters under equal ripple requirement. Moreover, single-phase full-bridge inverters for each phase are found to provide the lightest weight in this design owing to the high fundamental output frequency, in keeping with the results of

[7]. Accordingly, the proposed drive is based on sets of single-phase full-bridge inverters driving independent phase windings of the three-phase machine.

The three-phase machine stator consists of ten sectors, each sector comprising three separate (open-ended) single-phase windings spanning a pole pair of a ten-pole-pair 1-MW permanent magnet machine (see [8] for details of the 1-MW machine design). Accordingly, a distributed power conversion system comprising ten 100-kW inverter sets is implemented, with each inverter set comprising three single-phase full-bridge converters with their dc inputs closely coupled. Each inverter set drives the three separate phase windings in a sector of the machine. The hardware of the presented 1-MW distributed power converter is shown in Fig. 1. The (a) side and (b) top (axial) views of the axially-air-cooled distributed power converter are shown with the inverters arranged radially in a decagonal pattern and coaxially-with a 1-MW machine.

The contributions of this paper are threefold. The distributed conversion approach offers a number of advantages, including improved weight and efficiency, simplified packaging and cooling, modularity and maintainability, and the flexibility to integrate the power electronics closely with the electric machine. The inverter sets were co-optimized with the electric machine and their respective thermal management systems to maximize the specific power of the overall 1-MW system [9]. (For detailed information on the different components of the 1-MW motor drive technology demonstrator, please refer to the companion papers in [8–11].) Furthermore, the distributed conversion system is air-cooled (by axial-air-flow), leveraging the abundance of cooling air available in the proposed system. The proposed 1-MW power converter system provides an enviable specific power of 53 kW/kg (which may be compared with other state-of-the-art high-power inverters in this space in Table 1).

Table 1   Megawatt-class, high-power-density converters for aircraft propulsion applications

	GE	Nottingham	UTK	MIT
Reference	[1]	[2]	[3]	This work
Rated Power	1 MW	4 MW	1 MW	1 MW
Machine winding	Single three-phase winding[†]	8× isolated wye-connected three-phase windings	Single wye-connected three-phase winding	10×, 3× separate single-phase windings
DC bus voltage AC phase voltage	2.4 kV$_{dc}$ 1650 V$_{rms}$	3 kV$_{dc}$ 404 V$_{rms}$	1 kV$_{dc}$ 388 V$_{rms}$	720 V 480 V$_{rms}$
Topology	3L-ANPC[‡]	8× 3L-ANPC	2 Interleaved 3L-ANPC	10× 3× Full-bridge
Switch Tech. Packaging	Si IGBT + SiC power modules	Si IGBT power modules	SiC power modules	SiC discrete
Machine's fund. elect. frequency	1.4 kHz	1 kHz	3 kHz	2.08$\bar{3}$ kHz
Device switching freq. Carrier ratio	20 kHz 14.286	15 kHz 15	60 kHz 20	80 kHz 38.4
Cooling	Water-cooled	Liquid-cooled	Cryogenically-cooled (nitrogen liquid/gas)	Air-cooled
Specific power	15 kW/kg	16.6 kW/kg	18 kVA/kg	53 kW/kg[§]
Efficiency	99.1%	98.5%	98.5%	>98%
Test Status	Verified (1 MW)	Partially verified (1 MW)	Verified (1 MVA)	Partially verified (inductive test)
SP Calc. (kW/kg)	Incl. structure, excl. coolant + heat-exchanger (HEX)	Excl. structure, coolant + HEX	Excl. enclosure, coolant + HEX weights	Incl. boards (Fig. 1), excl. cooling fans + enclosure

[†]The test motor three-phase winding configuration, wye or delta-connected, is not provided in [1].

[‡]Three-level Active Neutral Point Clamped (3L-ANPC)

[§]The anticipated specific power is 38 kW/kg when the weight of the 30 boards and air-cooling source are considered, while excluding the enclosure. When the enclosure is included and air-cooling source is excluded, the anticipated specific power is 27 kW/kg. When all components are taken into account in the test setup for one 100-kW full-bridge inverter set, including the air-cooling source and structure, the calculated specific power is 22 kW/kg. It is worth mentioning that neither the air-cooling source nor the enclosure in the test setup were optimized for weight; they were solely used for preliminary testing purposes.
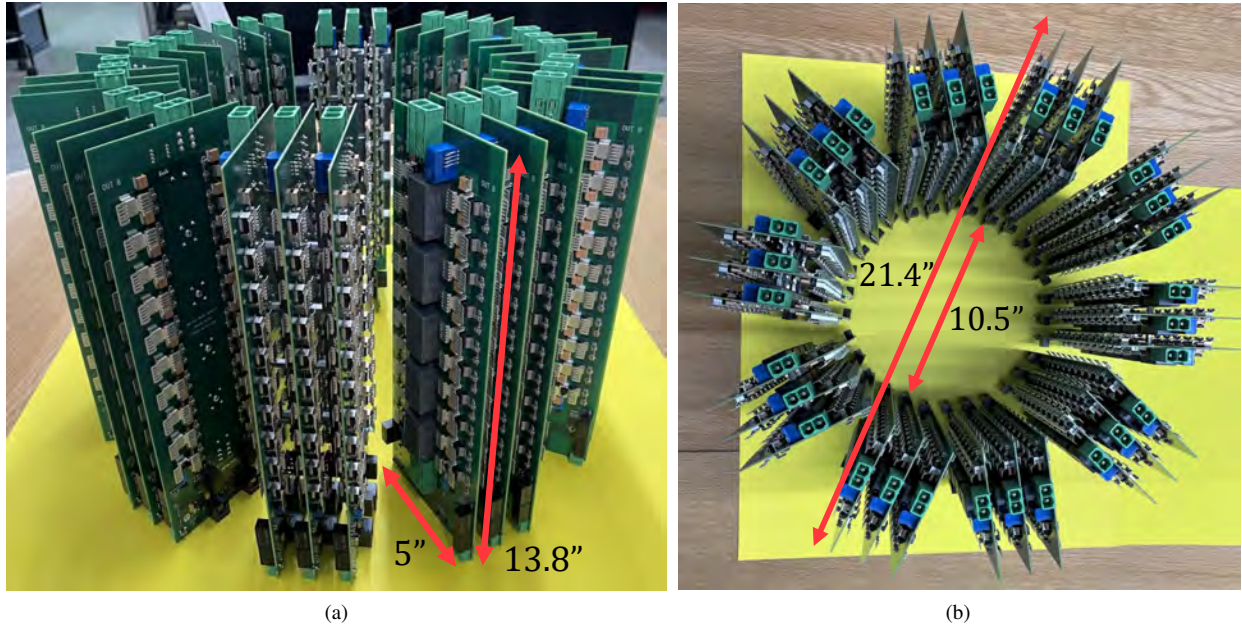
Fig. 1 Air-cooled 1-MW inverter system based on distributed power conversion. The full inverter system comprises ten 100-kW inverter sets, with each inverter set comprising three single-phase full-bridge inverters with tightly-coupled dc inputs. The inverters are designed to be arranged radially in a decagonal pattern and coaxially with (and in close proximity to) a 1-MW machine. (a) side view and (b) top view as seen into the axial dimension of the motor drive.

II. Topology Selection

The work in [7] compared the performance of the three-phase bridge inverter to a group of three single-phase full-bridge inverters for motor drive applications. It was found that for a given semiconductor device area and equal rms phase current ripple, separate full-bridge inverters are preferable for designs in which switching losses are dominant, whereas three-phase inverters are preferable for designs in which conduction losses are dominant. Individual phase drive is thus desirable in applications requiring high switching frequencies, as in high-speed low-inductance machines. This result motivated the authors to consider use of single-phase full-bridge inverters in the proposed design.

The main design objective of the 1-MW drive is maximizing its specific power (including the weight of the electric machine, power electronics and thermal management system) while maintaining adequate efficiency and cooling. To achieve this, an efficiency-weight comparison is performed considering inverter sets based on two-level topologies as well as a multilevel topology that is often favored in this application. Specifically, the three topologies are: (a) a group of three full-bridge inverters driving a machine with open-ended windings (Fig. 2(a)); (b) a three-phase bridge inverter driving a machine with delta-connected windings (Fig. 2(b)); and (c) a three-phase, three-level ANPC inverter driving a machine with delta-connected windings (Fig. 2(c)). (The particular phase winding configuration for three-phase inverters is not fundamental to the inverter comparison, but avoids rescaling machine turns between the three-phase bridge inverter and single-phase inverters.) As will be detailed in this section, the topology comparison reveals that even though multilevel inverters achieve the highest efficiency, they are by far the heaviest in weight. By comparison, groups of single-phase full-bridge inverters achieve the lightest weight and the second highest efficiency of the three considered options.

An example 1-MW machine with sets of three-phase-connected windings or three open-ended windings was used as the load (Table 2). This machine design is based on the outcome of the co-optimization routine described in [9]. However, the topology comparison result is not affected by modest changes in the machine design. In particular, the machine has ten electrically-separate sectors, each sector consisting of a group of three open-ended single-phase windings comprising a three-phase set, or a set of three-phase delta-connected windings. The 1-MW inverter system is divided into ten 100-kW three-phase inverters based on one of the considered inverter topologies in Fig. 2, with each of the ten inverter units driving a sector of the machine. Performance comparisons among inverters are made based on a
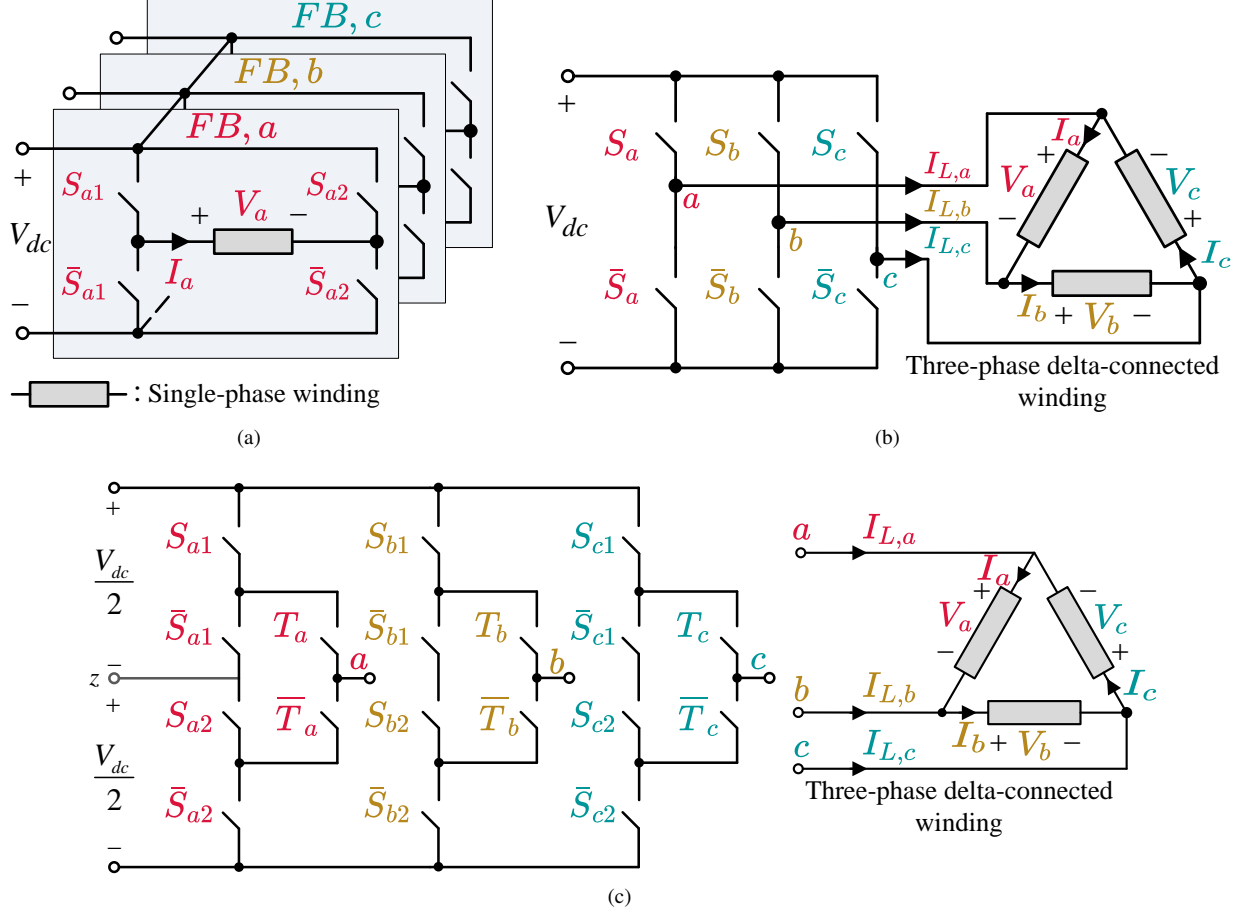
Fig. 2 **The three inverter topologies under consideration: (a) a set of three single-phase full-bridge inverters driving a machine with open-ended windings, (b) a three-phase bridge inverter driving a machine with delta-connected winding, and (c) a three-phase ANPC inverter powering a machine with delta-connected winding.**

specified rms phase current ripple percentage (e.g. 2.7%) to impose identical high-frequency losses in the machine; this implies different required switching frequencies of the different topologies (e.g., as detailed in [7]). A comparison among available GaN and SiC discrete devices and SiC power modules was made and the selected highest-performing devices were used in the design co-optimization and comparison studies under the assumption that the device area used could be freely scaled. An inverter design based on the 1200-V SiC C3M0075120J MOSFET was chosen for the 1-MW system design as it offered the highest performance among available devices and modules.

A. Assumptions

The following assumptions are made in the inverter topology comparison. The total loss of each of the respective 1-MW inverters includes the losses of FETs, gate drivers, and high-frequency capacitors, while the total mass includes the total weight of FETs, gate drivers, high-frequency capacitors, circuit boards, and heatsink. A heatsink with a mass-loss ratio of 0.634 kg/kW was considered in the topology comparison. The gate driver chips are assumed to have half the footprint area as the FETs. The weight of the printed circuit boards (PCB mass denoted as M_{PCB}) for each of the respective topologies is estimated by multiplying the total component area (including the area of the FETs, gate drivers, and high-frequency capacitors) by a mass-to-area density factor and a space factor of 1.5 as the following:

$$M_{PCB} \approx 1.5 \times \rho_{PCB} \times (A_{tot}) \tag{1}$$

where M_{PCB} is the estimated total PCB mass and $A_{tot} = A_{FETs} + A_{GDs} + A_{HF-Caps}$ is the total component area including the area of the FETs (A_{FETs}), gate drivers (A_{GDs}), and high-frequency capacitors ($A_{HF-Caps}$). In (1), a

Table 2 1-MW permanent magnet machine design specifications (used as an example for the topology comparison).

	Power	Speed	Pole pairs (# of multiphase windings)	Output frequency	Mod. index	RMS current ripple ratio
	1 MW	12500 rpm	10	2083.$\bar{3}$ Hz	0.927	2.7%
Topology	winding config.	DC bus voltage	Terminal inductance / Terminal resistance	Back-emf voltage (Fund.)	Phase current (Fund.)	Output phase voltage (Fund.)
3-phase bridge	3-phase delta	720 V	116.6 μH / 42.4 mΩ	455.3 V$_{rms}$ (643.9 V$_p$)	73.5 A$_{rms}$ (104 A$_p$)	472 V$_{rms}$ (667.5 V$_p$)
Full-bridge	3× single-phase	720 V	116.6 μH / 42.4 mΩ	455.3 V$_{rms}$ (643.9 V$_p$)	73.5 A$_{rms}$ (104 A$_p$)	472 V$_{rms}$ (667.5 V$_p$)
3-phase ANPC	3-phase delta	1200 V	324 μH / 117.9 mΩ	758.9 V$_{rms}$ (1073.3 V$_p$)	44.1 A$_{rms}$ (62.4 A$_p$)	786.7 V$_{rms}$ (1112.6 V$_p$)

PCB mass-area density of $\rho_{PCB} = 0.9584 \times 10^{-3}$ kg/cm^2 is estimated as an upper limit (using a PCB weight estimator [12]) by assuming a four-layer board and conservative PCB specifications, such as copper thickness of 140 μm (4-oz copper), 100% copper density and carrier thickness (FR4) of 2mm.

1. Devices

The topology comparison is performed with the preferred 1200-V SiC MOSFET C3M0075120J. MOSFETs are derated to 60% of the maximum device voltage in the full-bridge and three-phase bridge inverters, whereas they are derated to 50% for the ANPC inverter to accommodate for non-idealities such as DC bus imbalance. For the ANPC inverter, the machine's number of series-connected turns per pole pair (and per phase) is scaled appropriately to utilize the available voltage. For example, in the machine design in Table 2, the number of turns is scaled by a factor of $V_{dc,3L}/V_{dc,2L} = 1200/720$ or equivalently the impedance is scaled by $(1200/720)^2$. Furthermore, we assume that the same device technology (C3M0075120J) is used for both the low-frequency and high-frequency device pairs in the ANPC inverter.

We summarize the device total loss assumptions (conduction loss plus switching loss) as follows: For the device conduction loss, an on-state device resistance of $R_{ds,on}|_{T_j=150°C} = 100m\Omega$ at $150°C$ maximum junction temperature is used as a conservative assumption for a single (unit) device. More details on the calculation of the total device conduction losses for the full-bridge inverter and three-phase bridge inverter can be found in [7]. The total device conduction loss for the three-phase ANPC inverter with delta-connected winding is similar to that of the full-bridge inverter as two devices carry the current at any time, assuming that the ANPC's low-frequency device uses the same device technology (i.e. C3M0075120J) and has the same semiconductor device area.

For the switching losses, the devices are assumed to be hard-switched. The switching loss in one half-bridge over a switching cycle comprises the turn-on and turn-off losses in the active (positive-current-carrying) and freewheeling (negative-current-carrying) devices, and is generally dominated by the active device. The total switching loss in a half-bridge can be estimated as some factor between 1 and 2 times the active device switching loss (we refer to this factor as k_l). For the topology comparison example provided in this paper, the switching loss in one half-bridge is assumed to be 2× the active device switching loss as a conservative assumption (the freewheeling device is assumed to have the same switching loss as the active device).[¶] To estimate the switching loss for a single device, we use the average total switching energy loss $\left\langle e_{sw,tot}(i_{ds}(t))|V_{dc}\right\rangle$ over one fundamental line cycle. This involves scaling the switching energy loss curves provided in the device datasheet. To account for the effect of junction temperature rise on the device switching loss, we apply a temperature correction factor of $k_T = E_{sw}|_{Tj=150°C}/E_{sw}|_{Tj=25°C} = 1.34$, as extracted from the datasheet. This factor corresponds to a maximum temperature rise of 125°C from room temperature, which we consider a conservative assumption. In contrast to the three-phase bridge and full-bridge inverters, the ANPC inverter has three devices connected to the output switching node at all times, leading to an additional C_{OSS} loss. As a result, we account for an extra switching loss component (E_{OSS}) when analyzing the ANPC inverter.

[¶]We measured k_l to be 1.3 in our experimental setup with the preferred switch (C3M0075120J) after implementing the inverter hardware. Changing k_l from 2 to 1.3 has an identical effect on all the considered inverter topologies and does not affect the outcome of the topology comparison. However, once the preferred inverter topology is chosen, it is beneficial for the designer to use a more accurate estimate of k_l for a specific device and experimental setup. Doing so can yield a closer estimate of the minimum-loss number of devices per switch position for a given inverter topology.

2. High-Frequency Capacitors

The high-frequency dc link capacitors are responsible for filtering the high frequency component reflected on the dc bus voltage. The high frequency component is effectively equal to the device average switching frequency for the three-phase bridge inverter, while it is equal to the ripple frequency or twice the average device switching frequency for the full-bridge inverter and three-phase ANPC inverter. To size the high-frequency dc bus capacitors and calculate the required area and weight, a 3% peak-to-peak dc bus voltage switching ripple is considered. A study was conducted to compare the performance of high-frequency capacitors, including aluminum electrolytic capacitors, film capacitors, and multi-layer ceramic capacitors (MLC). The study found that MLC capacitors have the highest specific power and power density, the lowest footprint area, a high rms current ripple rating, a relatively high voltage rating, and relatively low ohmic losses (lower than aluminum electrolytic capacitors but higher than film capacitors). Based on this study, a ceramic capacitor B58035U9255M00 from the CeraLink series of TDK was selected and adopted for sizing the high-frequency capacitors in the topology comparison study. Three-level carrier-based modulation schemes have been adopted in sizing the high-frequency dc bus capacitors. This assumption corresponds to three-level line-line output voltage in the three-phase bridge and full-bridge inverters, and five-level line-line output voltage in the three-phase ANPC inverter. Therefore, the required capacitance per phase considering 50% duty ratio for maximum voltage ripple can be written as:

$$C_{dc,HF} = \frac{I_o}{4\Delta v_{c,pp} f_{HF}} \tag{2}$$

Here, I_o is the fundamental peak line current for the three-phase bridge and three-phase ANPC inverters, whereas it is the fundamental peak output phase current for the full-bridge inverter. The frequency is given as $f_{HF} = f_{sw}$ for the three-phase bridge inverter, whereas it is given as $f_{HF} = f_{ripple} = 2f_{sw}$ for the full-bridge and three-phase ANPC inverters. $\Delta v_{c,pp}$ is the maximum voltage ripple on the dc bus, e.g., $\Delta v_{c,pp} = 3\% V_{dc}$ for the example topology comparison in this paper. We note that we neglect any low-frequency (e.g., twice-fundamental-frequency) ripple in the bus capacitors. This pertains to the case of three single-phase inverters because it is assumed that a given set of three single-phase inverters has their dc bus inputs tightly coupled such that low-frequency pulsations cancel among the inverter inputs.

B. Motor Drive Simulation Results

For a fair comparison, the three topologies are compared under equal-phase-current rms ripple. Equivalent carrier-based pulse-width-modulation (PWM) schemes are adopted to find the average device switching frequency required to achieve a specified percentage rms ripple in the machine phase-currents (i.e. 2.7%). Namely, (a) three-phase sine-triangle PWM is used for the full-bridge drive and (b) a PWM with triangular carrier and one-sixth third-harmonic-injected references is used for the three-phase bridge inverter with delta-connected winding (three-level switched output voltage). For the three-level ANPC inverter with delta-connected winding, (c) three-level phase disposition (PD) PWM with in-phase triangular carriers (above and below the reference zero point) and one-sixth third-harmonic-injected references are used (five-level switched output voltage). As shown in [7], the device average switching frequency for the full-bridge and three-phase bridge inverters can be found analytically or by simulation. Here, we use simulation to find the device average switching frequency for equal-phase-current rms ripple percentage in the respective inverter topologies. It is found that for 2.7% phase-current rms ripple the full-bridge drive requires 79.17 kHz, while the three-phase bridge inverter requires 129.17 kHz and the three-phase ANPC inverter requires 29.17 kHz. The required device average switching frequencies for each topology are summarized in Table 3.

Table 3   Required device average switching frequency for each of the respective inverter topologies to achieve 2.7% phase-current rms ripple for the 1-MW motor drive design (given in Table 2).

	Full-bridge inverter	Three-phase bridge inverter	Three-level ANPC
Carrier ratio (f_c/f_o)	38	62	28
Device switching frequency (f_{sw})	$= 38 \times f_o = f_c$ $= 79.17$ kHz	$= 62 \times f_o = f_c$ $= 129.17$ kHz	$= 14 \times f_o = f_c/2$ $= 29.17$ kHz

A 100-kW three-phase set (one of the ten three-phase sets in the 1-MW drive) of each inverter topology is simulated

with the corresponding average device switching frequency (Table 3) with the machine parameters specified in Table 2. Simulated current waveforms for the full-bridge, three-phase bridge, and three-phase ANPC drives are shown in Figs. 3(a)-3(c), respectively. The simulated phase-current rms ripple percentages for the full-bridge inverter, three-phase bridge inverter, and three-phase ANPC inverter are 2.67%, 2.65%, and 2.73%, respectively. This confirms that the average device switching frequency for each of the considered inverter systems achieves the motor design specified rms current ripple percentage.
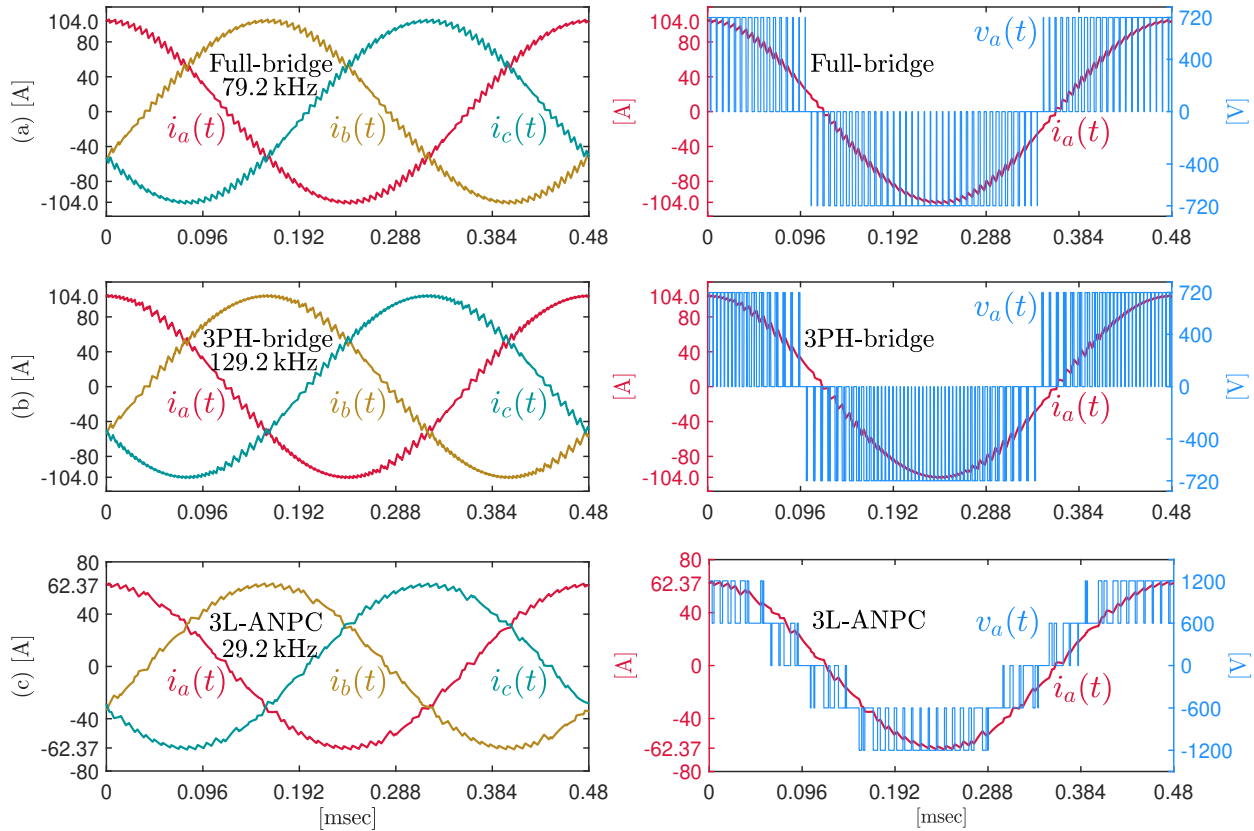

Fig. 3 **Simulated phase current waveforms (left-hand-side figures) and phase-A voltage/current waveforms (right-hand-side figures) are shown for the (a) full-bridge inverter, (b) three-phase-bridge inverter and (c) three-phase ANPC inverter, from top to bottom, respectively. The simulated phase-current rms ripple percentages for the full-bridge inverter, three-phase bridge inverter, and three-phase ANPC inverter are ~ 2.7% with device average switching frequencies of 79.2 kHz, 129 kHz, and 29.2 kHz, respectively.**

C. Total Loss Versus Total Weight

In the efficiency-weight comparison, the total loss of the 1-MW inverters accounted for the total device loss (conduction and switching), high-frequency capacitor losses for a specified peak-peak dc bus voltage ripple, and the gate driver losses. The total weight, on the other hand, included the weight of FETs, gate drivers, heatsinks and the dc bus high-frequency filtering capacitors. The total loss versus weight curve comparing the three different converters is shown in Fig. 4. As seen from the figure, the multilevel drive is the most efficient as compared to the full-bridge and three-phase bridge drives; this is due to the reduced device switching frequency and thus switching losses for equal percent rms phase-current ripple. However, it is by far the heaviest in weight owing to the relatively large high-frequency bus capacitance required for equal dc voltage ripple. By contrast, a group of full-bridge inverters yields by far the lightest weight and the second-highest efficiency of the three options, making it the preferred choice.

7

D. Optimum Number of Devices Per Physical Switch Position of the Selected 1-MW Full-Bridge Inverter System

With the selected 1-MW full-bridge inverter system in the above comparison, we plot the total loss (comprising losses from device conduction, device switching, gate drivers and high-frequency dc bus capacitors), and the individual loss components against the normalized semiconductor device area per switch position (equivalently, the total number of C3M0075120J devices per switch) in Fig. 5. The minimum-loss (highest-efficiency) point, minimum-weight point point, and the selected design point are also marked in the chart. Ten FETs per switch is selected as the design point for each single-phase inverter which is closer to the maximum-efficiency point than to the maximum-specific-power point to provide additional thermal device margin for the inverters.$^{\parallel}$
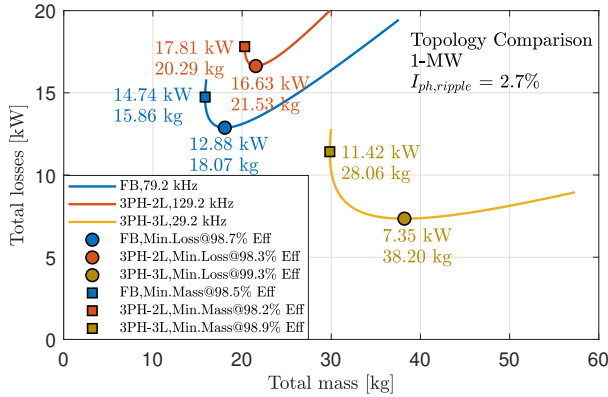

Fig. 4   Total loss versus total mass curve of the 1-MW distributed full-bridge, three-phase bridge and three-phase three-level ANPC inverters.
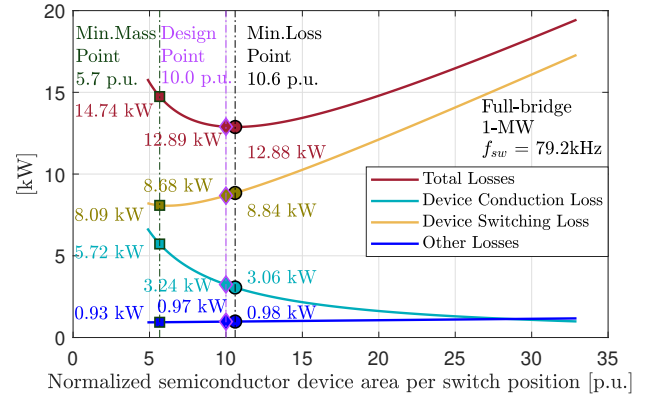

Fig. 5   Total loss versus normalized semiconductor device area per physical switch position of the 1-MW distributed full-bridge inverter.
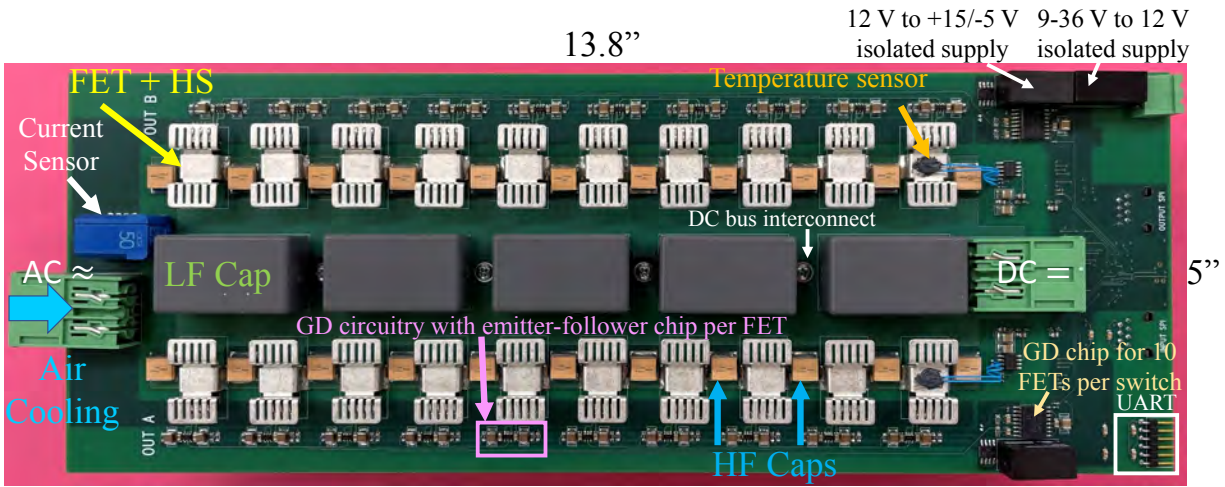
III. Inverter Hardware

A. Overview

As part of the co-optimization process described in [9], we swept the device switching frequency between 20 kHz and 100 kHz in the co-optimization loop to identify the highest specific-power full-bridge-inverter-based motor drive design. Our co-optimization process identified an optimum device switching frequency of 80 kHz. The number of devices per switch was chosen through an optimization process (which was part of a co-optimization routine alongside the electric machine and thermal management subsystems) that minimized the total full-bridge inverter system loss as a function of the normalized semiconductor device area and device switching frequency. We selected the final number of devices per switch per single-phase inverter between the minimum-mass point and the minimum-loss point, closer to the maximum-efficiency point (i.e., 10 FETs per switch), to provide additional design thermal margin for the inverters (see Fig. 5).
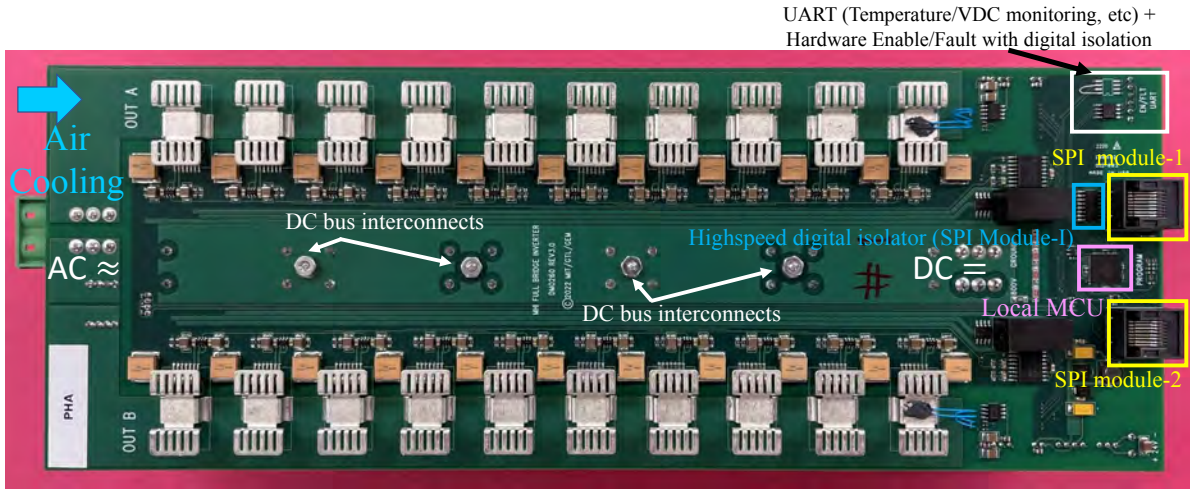
Top and bottom views of one 33.3-kW single-phase full-bridge inverter are shown in Fig. 6 (high-side FET view Fig. 6(a) and low-side FET view Fig. 6(b)). Each switch position has ten parallel 1200-V SiC devices (CREE C3M0075120J) based on the co-optimization results. A picture of one 100-kW inverter set comprising three full-bridge boards is shown Fig. 6(c). The key components of each 33.3-kW full-bridge board are summarized in Table 4. It was found in lab experiments that the FETs that are farthest from the cooling source have the highest operating junction temperatures. Thus, resistance temperature detectors (RTDs) are glued with low thermal-resistance epoxy to the heatsinks of the four devices farthest from the cooling source as seen in Figs. 6(a)-6(c).

The mass of the inverter set as seen in Fig. 6(c) (including the input and output connectors which are not shown in the figure) is 1.87 kg. The mass of the enclosure is 1.837 kg, whereas the mass of the cooling fans is 0.777kg. It is worth noting that the enclosure and fans were not optimized for minimum weight, and used only for testing an inverter set.

$^{\parallel}$The furthest points to the left of the curves in Fig. 4 and Fig. 5 represent the theoretical device thermal limits.

Fig. 6 Hardware pictures in (a) and (b) show the high-side and low-side FET views of one 33.3-kW single-phase full-bridge board, respectively, whereas the picture in (c) shows a top view of one 100-kW full-bridge inverter set.

Table 4   Key components of of each of the 30 33.3-kW full-bridge boards

Component	MOSFET	Gate Driver	HF Capacitor	LF Capacitor	Heatsink
Part no	C3M0075120J	UCC21750DW (per switch), ZXGD3006E6QTA (emitter follower per FET)	B58031U9254M062	C4AQQLW4500A33J	7106DG
Qty per 1-phase inverter	×40	×4 ×40	×44	×5	×40

B. Key Features

The dc bus of the three full-bridge boards is tightly electrically coupled (through aluminum interconnect standoffs) to provide a low-impedance path for cancellation of twice-line-frequency energy-pulsation components. Additionally, the high-side and low-side FETs of a single-phase board's half-bridge are overlaid on the top and bottom sides of the board, respectively. This layout approach, as opposed to having the FETs on the same PCB plane, minimizes switching commutation loops, resulting in low switching over-voltage. The gate driver chips for each FET, including the high-side FETs, are located over copper planes which have the same voltage as the MOSFET's source pins (output phase copper trace for the high-side FET, and ground copper trace for the low-side FET). This approach simplifies driving the high-side FETs, eliminates the need for complicated gate driver circuitry, and ensures safe and reliable device operation. To enhance signal integrity and reduce common-mode noise, a local microcontroller supplies the gate signals for each board.

C. Controls

A three-level carrier-based modulation scheme is employed for the full-bridge inverter system. Each single-phase board is equipped with a local microcontroller, specifically the dsPIC33EV64GM006 digital signal controller (DSC) from Microchip. The processors run with an instruction cycle rate of $F_{CY} \approx 60$ MHz (60 MIPS) and generate carriers at a rate of 120 MHz. Each set of three single-phase boards can be run in open-loop voltage control or closed-loop current control with the encoder angle and current or voltage commands received from a master controller board via an isolated serial-peripheral-interface (SPI) communication. The duty cycle commands are calculated on the phase-A DSC, and the boards are connected in a daisy-chain configuration using an isolated SPI. This interface is used to transfer the phase currents and PWM commands among the boards to allow closed-loop d-q current control to be used with each set of three single-phase boards. The SPI communication also facilitates synchronization of the boards to a single encoder signal and current or voltage command. Moreover, phase-locking of the central unit processors' (CPUs') clocks on the different inverter boards to the phase-A board has been implemented (phase-locking of clocks of multiple boards to a board, or to a master reference will be implemented when operating multiple inverter sets in the final system). Each board includes over-current protection, temperature monitoring of the four hottest FETs, and DC bus voltage monitoring. The overall controls diagram for one full-bridge inverter set is shown in Fig. 7.**

IV. Experimental Validation

A. Full-Bridge Inverter Test with Load Inductors

As the electric machine for the co-designed and co-optimized motor drive system is not yet complete (under construction at the time of writing) we have validated the performance of a full-bridge inverter set through reactive power testing using three inductors yielding equivalent voltage and current stress levels in the devices. The purpose of the test is to stress the MOSFETS at the same peak drain-source voltage and peak current at each switching cycle (or the same dc bus voltage and the same rated rms current over one complete line cycle) that they would see if they drove the 1-MW motor drive at full power (i.e. rated bus voltage and rated rms current). As a result, we expect that this test would incur approximately similar device losses for the full-bridge inverter set over one line cycle as that of the real 1-MW motor drive test.

The experimental setup of one full-bridge inverter set with three inductors shown in Fig. 8(a). The inverter set

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**The controls diagram is simplified and does not include hardware implementation details. It also omits the temperature and bus voltage monitoring through universal asynchronous receiver-transmitter (UART) protocol.
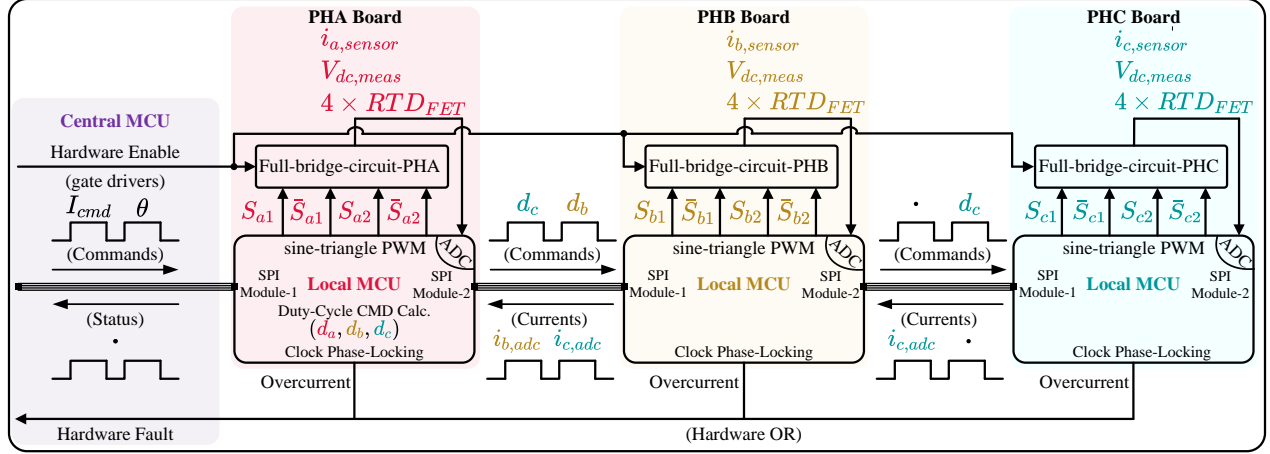
Fig. 7   Overall controls diagram of one 100-kW full-bridge inverter set.

is tested at 720 V_{dc} bus voltage and rated current of $\approx$ 74.6 A_{rms} in the phase inductors, whose phase impedance $\approx j120\mu H \times \omega_o + 0.05$ [Ω] (similar to that of the machine design in Table 2 without the phase back-emf voltages). The three-phase experimental waveforms of one full-bridge inverter set, which are operated with a 2 kHz fundamental output frequency and an 80 kHz switching frequency are shown in Fig. 8(b). It can be observed that the phase current waveforms are sinusoidal with a maximum measured rms ripple of 2.5%. The key parameters, operating conditions and performance specifications of the full-bridge inverter set three-phase experiment with three inductors are summarized in Table 5.

Table 5   Key experimental parameters and performance specifications of the full-bridge inverter set three-phase experiment with three inductors at 720-Vdc and 74.6-A$_{rms}$.

Rated Power	DC Bus Voltage	Fund. Line Frequency	Phase Inductance, Resistance	Fund. Phase Current	Fund. Phase Output Voltage
100 kW	720 V	2 kHz	120 μH, 50 mΩ	105.5 A_p	177.8 V_p (FFT of meas. PHA)
Operating Mod. Index	Device f_{sw}	Phase RMS Current Ripple ($I_{a,ripple}/I_a$)	Airflow rate (inverter set)	Max measured FET (RTD) $T_{heatsink}$	Max estimated operating $T_{junction}$
0.247	80 kHz	2.5% (max)	900 ft/min	72°C	105°C

To determine the system losses, the input dc power is measured with a WT1800 Precision Power Analyzer from Yokogawa. The inverter losses are estimated by subtracting the power dissipated in the load inductors from the input power. The inductor loss calculation include the fundamental-frequency and high-frequency core losses plus the fundamental winding losses (high-frequency winding losses are negligible of the single-layer litz windings of the inductors). The power measurements and loss estimation is summarized in Table 6.

Table 6   Estimated Losses of One Full-Bridge Inverter Three-Phase Set Operated at Rated Voltage and Current

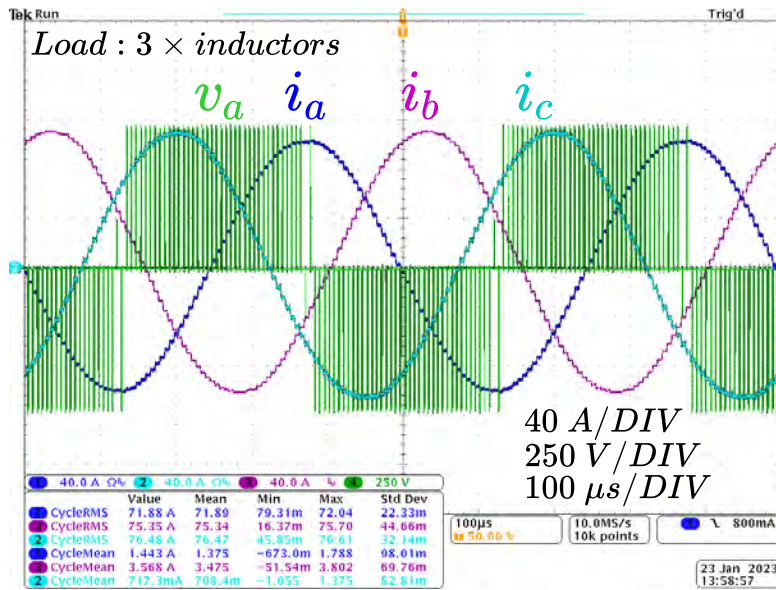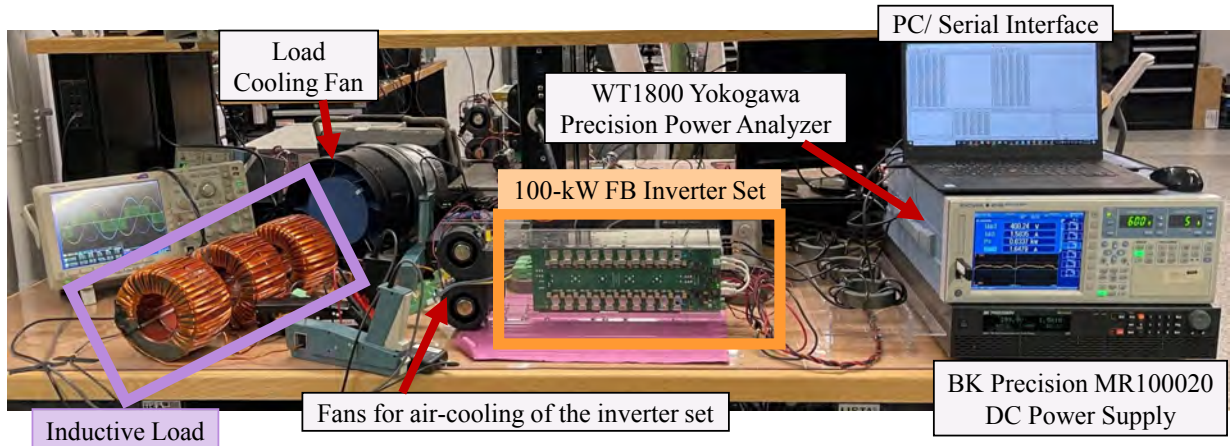| Measured Input Power (P_{IN})	Power Dissipated in Inductors ($P_{L,diss}$)	Total Loss, per FB inverter set ($P_{InvLoss}$)	Lumped Loss per FET ($P_{InvLoss}/120$)
2209 W	918 W	1291 W	10.8 W

Fig. 8 **(a) Experimental Setup and (b) voltage and current waveforms at 720 V_{dc} and $\approx$ 74.6 A_{rms} of a three-phase test with three load inductors. The imbalance in current amplitudes is attributed to slight variation among the load inductances.**

In Table 6, the projected total loss for ten full-bridge inverter sets operating with 720 Vdc and 74.6 Arms (i.e., stressing the devices at rated peak voltage and current per switching cycle) is 12.96 kW. The projected normalized total loss for 1-MW of power is thus 1.3%, suggesting an expected inverter efficiency of 98.7%. Note that this efficiency figure is only an expectation, as the efficiency operating at rated real power has not yet been obtained.

The thermal performance of the inverter has also been evaluated at 720 V$_{dc}$ and 74.6 A$_{rms}$. The airflow rate to maintain the optimum thermal performance of the MOSFET heatsinks is 800 ft/min. The cooling fans installed in the inverter set enclosure provide a minimum flow rate of 900 ft/min, which meets the rated airflow requirement. The RTD temperature of the heatsink of the hottest FET was measured as 72°C. In a separate experiment (not shown here) to characterize the thermal-resistance between the MOSFET tab and heatsink, thermocouples were soldered to both the tab and heatsink of a farthest FET from the air-cooling source to determine the thermal resistance between the tab (or "case") and heatsink. It was estimated (conservatively) that the tab-to-heatsink thermal resistance is approximately 1.9°C/W. With junction-to-case thermal resistance of 1.1°C/W of the 1200-V-C3M0075120J SiC devices, this amounts to an estimated junction-to-heatsink thermal resistance of 3°C/W. For the 10.8 W lumped loss per device (which is also a conservative estimate from Table 6), this results in about 32 °C temperature rise above the heatsink temperature, or equivalently, an operating junction temperature of 105°C (for the hottest FET). This suggests that there is 45°C thermal margin to the device maximum junction temperature limit (150°C) at the rated dc bus voltage and ac phase currents.

B. Full-Bridge Inverter Three-phase Test with a 9-Slot Stator Section

The full-bridge inverter set has also been tested with a three-phase 9-slot stator section. The purpose of this test is threefold: (a) to verify the full-bridge inverter performance driving a load with approximately the same impedance as that of the final stator, including similar terminal inductance, resistance, and capacitance; (b) to verify that there will be no significant line reflections at the machine terminals with the short similar terminal lead lengths to be used between the inverter and machine stator (i.e., ≤ one foot) in the final system; and (c) to verify the robustness of the machine insulation system under continuous operation of 720-V PWM waveforms with the operating dv/dt of the inverter output (greater than 45 kV/μsec of the implemented hardware in this paper).

A picture of the 9-slot stator section is shown in Fig. 9a. The three-phase winding of the 9-slot stator section consists of one multiphase winding subsystem (out of ten) comprising three separate single-phase windings and spanning one pole pair of the final 10-pole-pair machine (i.e. the 10-pole-pair machine in Table 2). Each single-phase winding comprises two series-connected five-turn coils with each phase coil spanning a pole. The wiring pattern and insulation system that is implemented in the 9-slot stator section is representative of those to be implemented in the final stator. Consequently, the three single-phase windings have a similar phase (terminal) inductance, resistance and capacitance, as well as a similar capacitance to core (ground).[††]

The terminal leads from the statorette to the single-phase inverters are ~ 1-ft long (> 30% longer than that of the final machine as a conservative test). Furthermore, two temperature sensor RTDs are inserted into two separate slots of the statorette as shown in Fig. 9(a) to monitor the windings' hot spot temperatures.[‡‡]

The experimental waveforms of one full-bridge inverter set driving the 9-slot stator section at 720 Vdc and ≈ 74.8 A$_{rms}$ (averaging the three-phase rms currents) are shown in Fig. 9(b). It can be observed that the phase currents are sinusoidal as expected, with a maximum measured phase current rms ripple of 2.7%. Furthermore, by examining the phase-a output voltage waveform, the switching over-voltage is less than 50 V above the rated 720 V$_{dc}$, which confirms that there are no significant line reflections. The experimental results of the inverter set with the stator section thus confirm that by having the inverters closely interconnected with the electric machine, line-reflection voltages can be avoided. Therefore, the proposed circumferential arrangement of the inverters physically and closely interconnected with the electric machine suggests that an output filter to limit dv/dt is not required.

We examine the behaviour of the RTDs while the inverter is operating at full voltage. The 9-slot stator section is attached through low-thermal resistance paste to an initial design fin-type heatsink (i.e. dummy heatsink not used in the final machine) for cooling while running the experiment at full voltage and near-rated rms phase current (Fig. 10(a)). Air-cooling is applied axially into the heatsink (air flows axially through the inner cylindrical region and the fin-region of the heatsink) and cools the stator section by conduction. The full-bridge inverter three-phase experiment with the heatsunk 9-slot stator section is run at 720 V$_{dc}$ and 63 A$_{rms}$ for a 40-minute long test. It is found that RTD temperature

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[††]A minor difference from the final system is that the 9-slot stator section is missing five-turn coils in the the first and last three slots which would be shared by neighboring sets of three single-phase windings in a complete 10-pole-pair stator. This asymmetry in the windings in the 9-slot stator section does not yield a major impact on the effective phase impedances.

[‡‡]A three-lead S1420PA120T625Z36 RTD and a two-lead S100725PDYT120B RTD from Minco are used to measure the winding temperatures inside the slots.
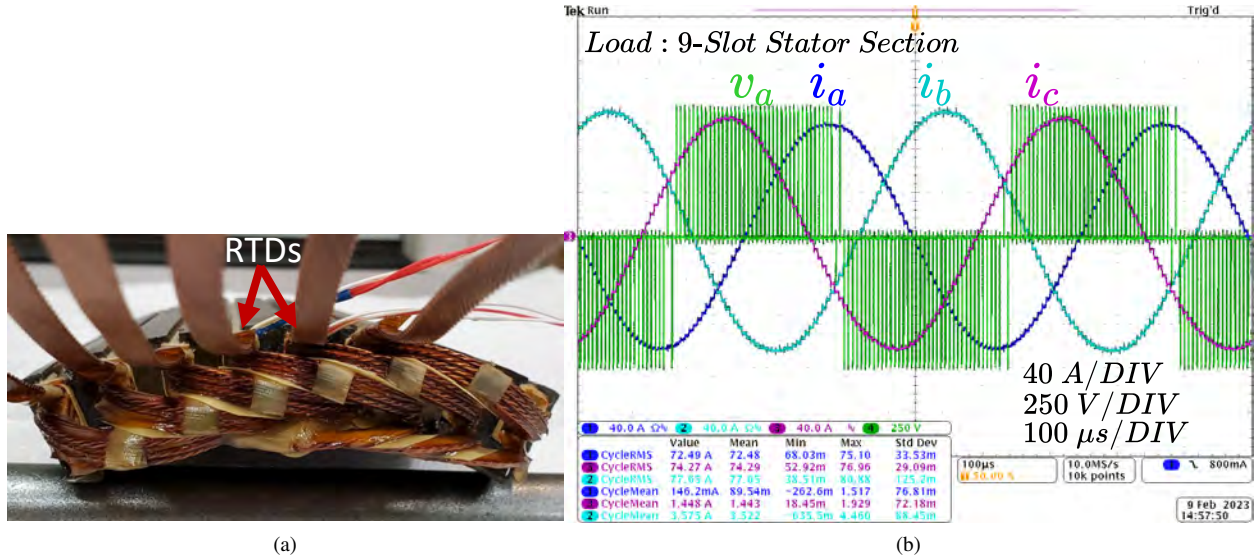
(a)   (b)

Fig. 9 **(a) This is an axial view of the 9-slot stator section after the winding process, installation of insulation and RTDs, and vacuum pressure impregnation are completed. (b) The picture shows voltage and current waveforms at 720 Vdc and $\approx$74.6 Arms of a three-phase test with three load inductors. The currents are unbalanced in amplitude, which is attributed to slight variations in the load inductances.**

readings are steady and noise free—unaffected by the inverter switching at full dv/dt as seen in Fig. 10(b). Taken together, the above results suggest that the close proximity of the inverters to the machine – enabled by their circumferential and axial placement – may obviate the need for filters between inverter and machine to address line reflections and electromagnetic interference (EMI).
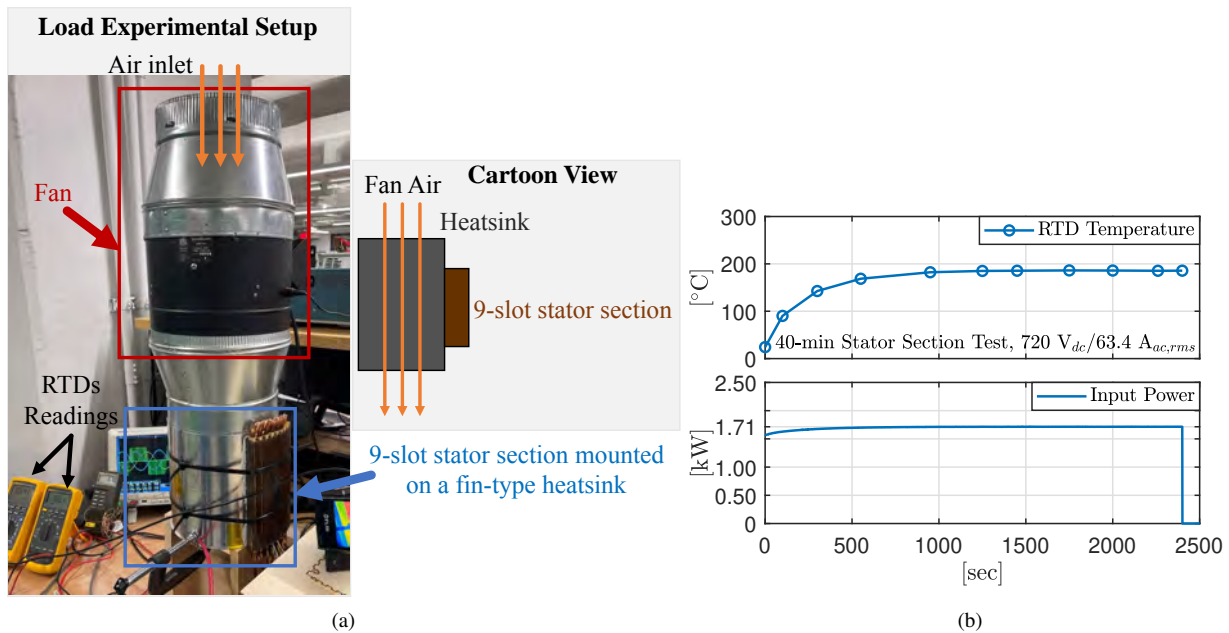

(a)   (b)

Fig. 10 **(a) The experimental setup for the 9-slot stator section in which the stator section is mounted on a test heatsink. In (b), a 40-minute data logging result of the temperature measured by one of the RTDs inserted in the stator slot, along with the input power measured by the WT1800 Power Analyzer, is shown for an ac current of 63.4 A$_{ac,rms}$.**

V. Conclusion

This paper summarizes major aspects of the design and optimization of an ultra-light inverter for a 1-MW motor drive. Distributed power conversion using a number of inverters sets to supply different sectors of the machine is valuable in achieving a high-specific-power motor drive design. The distributed conversion approach offers a number of advantages, including improved weight and efficiency, simplified packaging and cooling, modularity and maintainability, and the flexibility to integrate the power electronics closely with the electric machine. Furthermore, it is shown that in this application, three single-phase full-bridge inverters yields lower weight than the more efficient (and more complex) three-phase ANPC inverter and less efficient three-phase bridge inverter under equal ripple requirements; this makes sets of three single-phase inverters the preferred inverter choice. Optimization of various aspects of the distributed power conversion architecture yields a high specific power that is promising for future aircraft motor drives. Among these aspects are switch selection, topology selection, co-design and co-optimization of the power electronics with the electric machine and the associated thermal management system, and the close integration of full-bridge inverter sets with the electric machine. It is anticipated that this work can benefit the development of light, efficient high-power motor drives for aircraft applications.

Acknowledgments

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